

IN THE CLAIMS

Please amend claims 1, 4, 5, 13, 16, 17, and 27 as follows:

Claims 1, 4, 5, 13, 16, 17, and 27 have been amended as follows:

a1 1. (Amended) A computer-implementable method of performing modulo division, using a dividend N and an n-bit divisor D to produce a remainder R, said method comprising:

non-iteratively processing $N \bmod D$ to produce the remainder R, where $D=2^n-1$ and $0 < N < (D-1)^2$.

b4 4. (Amended) The computer-implementable method of claim 37, 5 further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

a2 5. (Amended) The computer-implementable method of claim 38, 11 further comprising the step of subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

a3 29 16. (Amended) The apparatus of claim 41, 23 said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

31
~~31~~. (Amended) The apparatus of claim ~~42~~³⁰, said apparatus subtracting the divisor D from the sum to produce the remainder R, if the sum is greater than the divisor D.

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~~21~~²⁷. (Amended) The apparatus of claim ~~13~~¹⁸, wherein said apparatus is a component of a Reed-Solomon coder.

Please add the following claims:

~~36~~³⁷. (New) The computer-implementable process of claim 1, further comprising the step of using said remainder R to perform Reed-Solomon coding of data on a computer.

T, 6150
AS
T, 0157
~~37~~³⁸. (New) The computer-implementable method of claim 1, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lfloor \frac{n}{2} \rfloor$ bits of the dividend N to produce the remainder R.

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~~38~~³⁹. (New) The computer-implementable process of claim ~~2~~⁷, further comprising the step of using said remainder R to perform Reed-Solomon coding of data on a computer.

T₁₀₁₆₀

T₁₀₁₆₁

¹¹
30. (New) The computer-implementable method of claim ²~~2~~, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lfloor \frac{n}{2} \rfloor$ bits of the dividend N to produce the remainder R.

¹⁷
40. (New) The computer-implementable process of claim ¹³~~3~~, further comprising the step of using said remainder R to perform Reed-Solomon coding of data on a computer.

T₁₀₁₆₂

²³
41. (New) The apparatus of claim 13, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lfloor \frac{n}{2} \rfloor$ bits of the dividend N to produce the remainder R.

T₁₀₁₆₄

T₁₀₁₆₅

³⁰
42. (New) The apparatus of claim ²⁵~~14~~, further the step of summing the upper $\lceil \frac{n}{2} \rceil$ and lower $\lfloor \frac{n}{2} \rfloor$ bits of the dividend N to produce the remainder R.

²⁸
43. (New) The apparatus of claim ²¹~~27~~, wherein said Reed-Solomon coder performs coding in data communication operations.

²⁹
~~44~~. (New) The apparatus of claim ²⁸~~25~~, wherein said Reed-Solomon
coder performs coding in data communication operations.

³⁷
~~45~~. (New) The apparatus of claim ³⁶~~26~~, wherein said Reed-Solomon
coder performs coding in data communication operations.

⁴⁰
46. (New) The apparatus of claim ~~32~~, said computer signal being
executed on a computer to perform Reed-Solomon coding of data.--
